What Is Claimed Is:

1. A cell element field for data processing, having function cell means for executing algebraic and/or logic functions and memory cell means to receive, store and/or output information,
wherein function cell-memory cell combinations are formed in which a control connection leads from the function cell means to the memory cell means.

2. The cell element field as recited in the preceding claim, wherein a processor, coprocessor and/or microcontroller forms a plurality of units such as function cells and/or memory cells whose function and/or interconnection is/are reconfigurable and/or preselectable.

3. The cell element field as recited in one of the preceding claims,
wherein the function cells are formed as arithmetic logic units.

4. The cell element field as recited in the preceding claim, wherein the arithmetic logic units are formed as extended ALUs.

5. The cell element field as recited in one of the preceding claims,
wherein the memory cells are designed as volatile and/or nonvolatile data memories.

6. The cell element field as recited in one of the preceding claims,
wherein the memory cells are designed for storage of data to be processed and/or program steps to be executed.

7. The cell element field for data processing,
wherein the memory cells are designed for sending stored

information directly and/or indirectly to a bus leading to the function cell in response to triggering by the function cell which controls them.

8. The cell element field as recited in one of the preceding claims,
wherein registers, in particular a backward register which is situated in the information path between the memory cell and function cell, are assigned to at least one memory cell and/or function cell.

9. The cell element field as recited in one of the preceding claims,
wherein the memory cell is situated to receive information from the function cell which controls it, an input-output cell and/or a cell having an arithmetic logic unit that does not control it.

10. The cell element field as recited in one of the preceding claims,
wherein at least one input-output means is assigned to the function cell-memory cell combination for sending information to an external unit and/or another function cell, function cell-memory cell combination and/or memory cell and/or for receiving information from it.

11. The cell element field as recited in the preceding claim, wherein the input-output means are also designed to receive control commands from the function cell.

12. The cell element field as recited in one of the preceding claims,
wherein the controller is designed to transmit at least some, preferably all of the following commands, and/or the memory cell and/or input-output cell is designed to decode the following commands: DATA WRITE/READ, ADDRESS

POINTER WRITE/READ, PROGRAM POINTER WRITE/READ, PROGRAM POINTER INCREMENT, STACK POINTER WRITE/READ, said commands in particular for internal and/or external access, PUSH, POP, OPCODE, FETCH.

13. The cell element field as recited in one of the preceding claims,
wherein the function cell as the sole master is able to access the control connection and/or the bus segment functioning as the control connection.

14. The cell element field for data processing as recited in one of the preceding claims,
wherein the function cell is situated adjacent to at least one memory cell and/or input-output cell.

15. The cell element field as recited in one of the preceding claims,
wherein the cell elements are arranged multidimensionally, in particular in a matrix, the function cell and/or the adjacent memory cell and/or input-output cell being able to receive data from an upper row and output data into a lower row, buses being provided in one row and the function cell and at least one memory cell and/or input-output cell being situated in one and the same row.

16. A method for operating a cell element field, in particular a multidimensional cell element field having function cells for execution of algebraic and/or logic functions and information providing cells, in particular memory cells and/or input-output cells for receiving and/or outputting and/or storing information,
wherein at least one of the function cells outputs control commands to at least one information-providing cell, **[the information]** is processed there in response to

the control command information for the function cell, and the function cell is designed to perform further data processing in response to the information provided from the information-providing cell in order to process data in the manner of a sequencer.

17. The method as recited in one of the preceding claims, wherein the function cell is designed **[to output]** at least some of the control commands
OPCODE FETCH,
DATA WRITE INTERNAL,
DATA WRITE EXTERNAL,
DATA READ INTERNAL,
DATA READ EXTERNAL,
ADDRESS POINTER WRITE INTERNAL,
ADDRESS POINTER WRITE EXTERNAL,
ADDRESS POINTER READ INTERNAL,
ADDRESS POINTER READ EXTERNAL,
PROGRAM POINTER WRITE INTERNAL,
PROGRAM POINTER WRITE EXTERNAL,
PROGRAM POINTER READ INTERNAL,
PROGRAM POINTER READ EXTERNAL,
STACK POINTER WRITE INTERNAL,
STACK POINTER WRITE EXTERNAL,
STACK POINTER READ INTERNAL,
STACK POINTER READ EXTERNAL,
PUSH,
POP,
PROGRAM POINTER INCREMENT
and in the course of cell element operation to output at least some, in particular all, of the control commands indicated above as necessary.